10.709Gb/s LASER DIODE DRIVER Chipset

Preliminary Technical Data — ADN2843

FEATURES

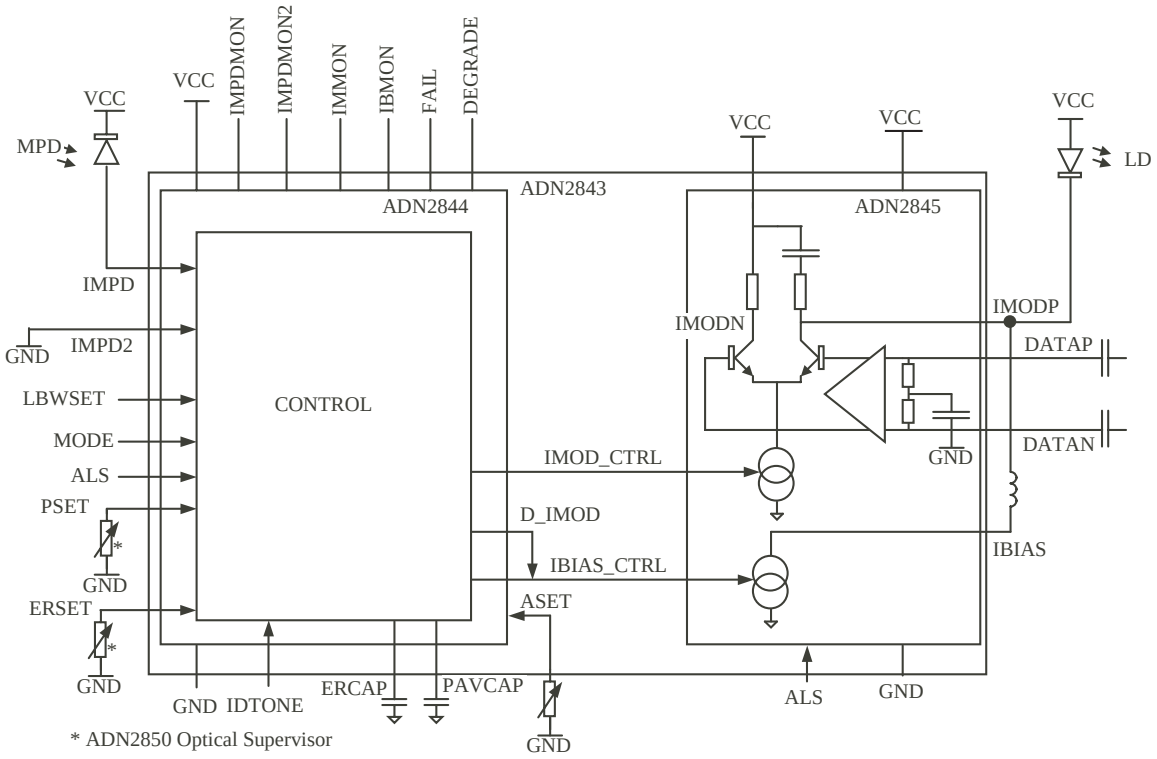
Data Rates from 50Mb/s to 10.709Gb/s
Typical rise/fall time 25/23 ps
Bias Current range 3mA to 80 mA
Modulation Current range 5mA to 80 mA
Monitor Photo Diode current 50μA to 1100μA
Closed Loop Control of both average optical power and extinction ratio
Laser fail and laser degrade alarms
Automatic laser shutdown, ALS
Dual MPD functionality for wavelength control
CML data inputs
50 Ω internal data terminations
+3.3V single supply operation
Driver supplied in dice format

APPLICATIONS

SONET OC-192, SDH STM-64
Suports 10.667Gb/s and 10.709Gb/s FEC rates
10Gb Ethernet IEEE802.3

GENERAL DESCRIPTION

The ADN2843 chipset uses a unique control algorithm to control both average power and extinction ratio of the laser diode, LD, after initial factory set-up. The chipset consists of two components. The ADN2844 contains the control loops, and the ADN2845 is the 10.7Gb/s data switch. The ADN2845 is available in dice format, and ADN2844 is available in packaged or dice format. External component count and PCB area are low as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life), and laser degrade (impending fail).



FUNCTIONAL BLOCK DIAGRAM

REV. PrD January 2003

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(V_{CC} = 3.0V to 3.6V, All specifications T_{MIN} to T_{MAX} unless otherwise noted. Typical values as specified at 25°C)

PARAMETER	Min	Typ	Max	Units	Conditions
LASER BIAS (BIAS)					
Output current Ibias	3		80	mA	
Compliance Voltage	1.2		Vcc-1.0	V	
Ibias during ALS			10	µA	see note#6
ALS shutdown response time			10	µs	
MODULATION CURRENT (IMODP, IMODN)					see note#1
Output Current Imod	5		80	mA	
Compliance Voltage	1.2		Vcc	V	
Imod during ALS			10	µA	
Rise time		25		ps	see note#7
Fall time		23		ps	see note#7
Random jitter		170		fs RMS	see note#2
Total jitter		7.41		ps Pk-Pk	see note#3
MONITOR PD (MPD,MPD2)					
Current	50		1200	µA	
Input voltage			1.6	V	
POWER SET INPUT (PSET)					
External capacitance			80	pF	see note#4
Voltage	1.15		1.35	V	
EXTINCTION RATIO SET INPUT (ERSET)					
Allowable Resistance Range	1k		25k	Ω	
Voltage	1.15		1.35	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.15k		13.5k	Ω	
Voltage	1.15		1.35	V	
Hysteresis		5		%	
CONTROL LOOP					
Time Constant		0.22		s	LBWSET= GND
		2.25		s	LBWSET = VCC
DATA INPUTS (DATAP,DATAN)					
Vp-p(single ended pk to pk)	300		800	mV	
Input impedance		50		Ω	
LOGIC INPUTS (ALS, LBWSET)					
Vih	2.4			V	
Vil			0.8	V	
ALARM OUTPUTS (Internal 30K to Vcc)					
Voh	2.4			V	
Vol			0.4	V	
IDTONE					
Fin	10		1000	KHz	
Input Current Range	50		4000	µA	
Voltage on IDTONE	Vcc-1.5			V	
IBMON,IMMON IMPDMON,IMPDMON2					
IBMON, IMMON Division Ratio		100		A/A	
IMPDMON,IMPDMON2		1		A/A	
IMPDMON to IMPDMON2 Matching			1	%	
Compliance Voltage	0		1.5	V	
SUPPLY					
Vcc	3.0	3.3	3.6	V	
Icc(ADN2844)		36		mA	see note#5
Icc(ADN2845)		75		mA	see note#5

Note 1: The ADN2845 high speed specifications are measured into a 5Ohm load.
Note 2: RMS jitter measured with a 0000 0000 1111 1111 repeating pattern at 10.7Gbps rate
Note 3: Peak-to-peak total jitter measured with a 2^13-1 PRBS with 80 CIDs pattern at 10.7Gb/s rate
Note 4: Max capacitance refers to capacitance of photo diode and other parasitic capacitance
Note 5: IBIAS=0, IMOD=0. See section on Power Dissipation for calculation of complete power dissipation
Note 6: In ALS mode approx. 15mA is sourced to the laser from the IBIAS pin which reverse biases the laser
Note 7: Using a 0.5nH ribbon between IMODP and the cathode of the laser diode

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{CC} to GND..... 5V
DataP to GND.....3.6V
DataN to GND.....3.6V
ALS to GND.....3.6V
IMOD_CONTROL to GND.....3.6V
IBIAS_CONTROL to GND.....3.6V
Operating Temperature Range
Industrial .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max).....+150°C

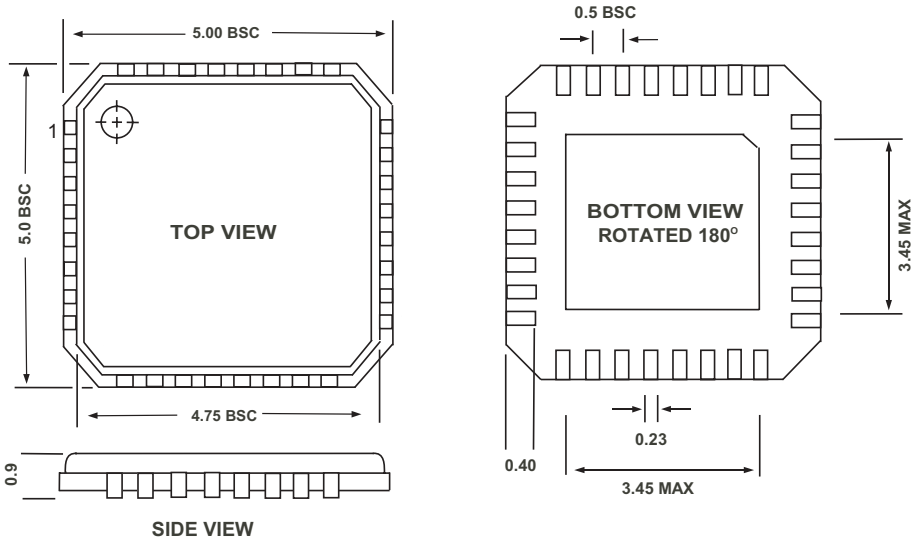
NOTES:
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Transient currents of up to 100mA will not cause SCR latch-up

Ordering Guide

Model	Temperature Range	Package Description
ADN284XXX(1) Chipset	-40°C to +85°C	ADN2844 Control loop: 32-Lead LFCSP ADN2845 Data Switch : Dice
ADN2843XXX(2)	-40°C to +85°C	ADN2844 Control Loop: Dice ADN2845 Data Switch: Dice

OUTLINE DIMENSIONS
Dimensions shown in mm

32-Lead(5x5) LFCSP (Exposed Paddle)
Exposed Paddle should be soldered to the most negative supply of the -ADN2844
(ADN2844 also available as bare die)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2841 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 2. Two key characteristics of this transfer function are the threshold current, Ith, and slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

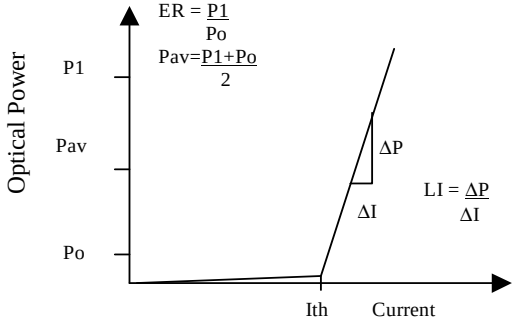


Figure 1. Laser Transfer Function

CONTROL

A monitor photo diode, MPD, is required to control the LD. The MPD current is fed into the ADN2841 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light to current (LI) slope (slope efficiency).

The ADN2843 uses automatic power control, APC, to maintain a constant power over time and temperature.

The ADN2843 uses closed loop extinction ratio control to allow optimum setting of extinction ratio for every device. Hence SONET/SDH interface standards can be met over device variation, temperature and time. Closed loop modulation control eliminates the need to either over modulate the LD or include external components for temperature compensation, thus reducing R&D time and second sourcing issues.

The ADN2843 dual loop control has three modes of operation. Each mode is given by the configuration of the MODE and D_IMOD pins as shown below:

Operation mode	MODE pin setting	D_IMOD pin connected to
A	HIGH	IBIAS
B	LOW	IBIAS_CTRL
C	LOW	IMOD_CTRL

Setting the ADN2843 in mode A(see figure2) allows operation with lasers which have LI non-linearity offering a better accuracy of the extinction ratio control. Care should be taken to ensure that the extra capacitance on the IBIAS pin due to the D_IMOD connection does not degrade the eye performance. When physical consraints doesn't allow a low capacitance interconnect between D_IMOD and IBIAS, the ADN2843 should be configured in mode B(see figure 3).

Configuring the ADN2843 in mode C allows operation without LI non-linearity compensation (see figure4). Average Power and Extinction Ratio are set using the PSET and ERSET pins respectively. A resistor is place between the pin and GND to set the current flowing in each pin. The internal control loops force the PSET and ERSET pins to 1.23V above GND.

The PSET resistor is given by the following formula:

$$R_{PSET} = \frac{1.23}{I_{av}} \quad (\Omega)$$

where I_{av} is average MPD current.

The value of the ERSET resistor is a function of the operation mode of the ADN2843 as follows:

For modes A and C,

$$R_{ERSET} = \frac{R_{PSET}}{2} \times \frac{ER+1}{ER-1}$$

For mode B,

$$R_{ERSET} = R_{PSET} \times \frac{ER+1}{ER-1}$$

Note that I_{ERSET} and I_{PSET} will change from laser diode to laser diode, therefore R_{ERSET} and R_{PSET} need to be adjusted for each laser diode. When tunning the laser diode, R_{PSET} should be adjusted first with R_{ERSET} at 25KΩ. Once the average power is set, R_{ERSET} is adjusted to set the desired extinction ratio. Once the values R_{PSET} and R_{ERSET} have been adjusted to set the desired average power and extinction ratio, the control loops maintain these values values of average power and extinction ratio over environmental conditions and time.

LOOP TIME-CONSTANT SELECTION

The control loop constant can be optimised for operation at data rates of 2.5GB/s and above by setting the LBWSET pin low. This results in a faster loop time constant. The required value for the PAVCAP/ERCAP capacitors in 22nF in this case.

For multi-rate operation, the LBWSET pin should be set high and the required value for the PAVCAP/ERCAP capacitors is 820nF. This results in a slower loop constant.

The PAVCAP/ERCA capacitors are connected between the respective pins and GND. The capacitors should be low leakagemulti-layer ceramic capacitors with an insulation resistance > 100GΩ or an RC > 1000s, whichever is the lower.

ALARMS

The ADN2843 alarms are designed to allow interface compliance to ITU-T-G958 (11/94) section 10.3.1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade). The ADN2843 has two alarms, DEGRADE and FAIL. These alarms are raised when IBIAS exceeds the respective DEGRADE and FAIL thresholds. These alarms are active high. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 1:100 to the FAIL alarm threshold.

The DEGRADE alarm will be raised at 90% of the FAIL threshold.

Example: I_{FAIL} = 50mA so $I_{DEGRADE}$ = 45mA

$$I_{ASET} = \frac{Ibiastrip}{100} = \frac{50mA}{100} = 500\mu A$$

$$**R_{ASET} = \frac{1.23\ V}{I_{ASET}} = \frac{1.23}{500mA} = 2.46\ k\Omega$$

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, eg. increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arise:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resultingin the MPD current dropping to zero. This gives closed loop feedback to the system that ALS has been enabled.

ALARM INTERFACE

The alarm voltages are open collector outputs. An internal pull up resistor of 30K is used to pull the logic high value to Vcc. However this can be over driven with an external resistor allowing alarm interfacing to non-Vcc levels. **Non-Vcc alarm output levels must be below the Vcc used for the ADN2843.**

MONITOR CURRENTS

IBMON, IMMON mirror the bias, modulation current at a ratio of 1:100 for increased monitoring functionality. IMPDMON and IMPDMON2 mirror the current in IMPD and IMPD2 respectively with a ratio of 1. All monitors source current from Vcc.

ID_TONE

The IDTONE pin is supplied for fibre identification/ supervisory channels or forcontrol purposes. This pin modulates the optical one level by adding a current to IMOD over a possible range of 2% of min Imod to 10% of max Imod. The ID_TONE current is set by an external current sink connected to the IDTONE pin. There is a gain of two between the IDTONE pin and the IMOD current. To ratio the IDTONE current to IMOD, the input current can be derived from the IMMON output current.

If the IDTONE function is not being used, this pin must be tied to properly disable it.

Note that using ID tones during transmission may cause optical eye degradation.

AUTOMATIC LASER SHUTDOWN

The ADN2843 ALS allows compliance to ITU-T-G958 (11/94), section 9.7. When ALS is asserted, both bias and modulation currents are turned off. In ALS mode approx. 15mA is sourced to the laser from the IBIAS pin which reverse biases the laser and ensures that it is turned off. Correct operation of ALS can be confirmed by the fail alarm being raused when ALS is asserted. Note this is the only time that DEGRADE will be low while FAIL is high.

Note: For correct ALS operation, ALS pin on ADN2844 and ADN2845 should both be driven.

DUAL MPD DWDM FUNCTION

The MPD function mirrors the current in MPD to the PSET pin and to the IMPDMON pin with a ratio of 1. If the IMPD monitor functionis not required, the monitor photo diode can be directly connected to the PSET pin, and the IMPD pin tied to GND. A second monitor photo diode can be connected to the IMPD2 pin. Its current is mirrored to IMPDMON2 and also to the PSET pin, where it is summed with the current mirrored from IMPD. The two MPD monitor currents can be used as inputs to a wavelength control function when used in combination with various optical filtering techniques. If IMPD2 pin is not being used, it should be tied to GND.

POWER DISSIPATION

The power dissipation of the ADN2845 can be calculated using the following expressions:

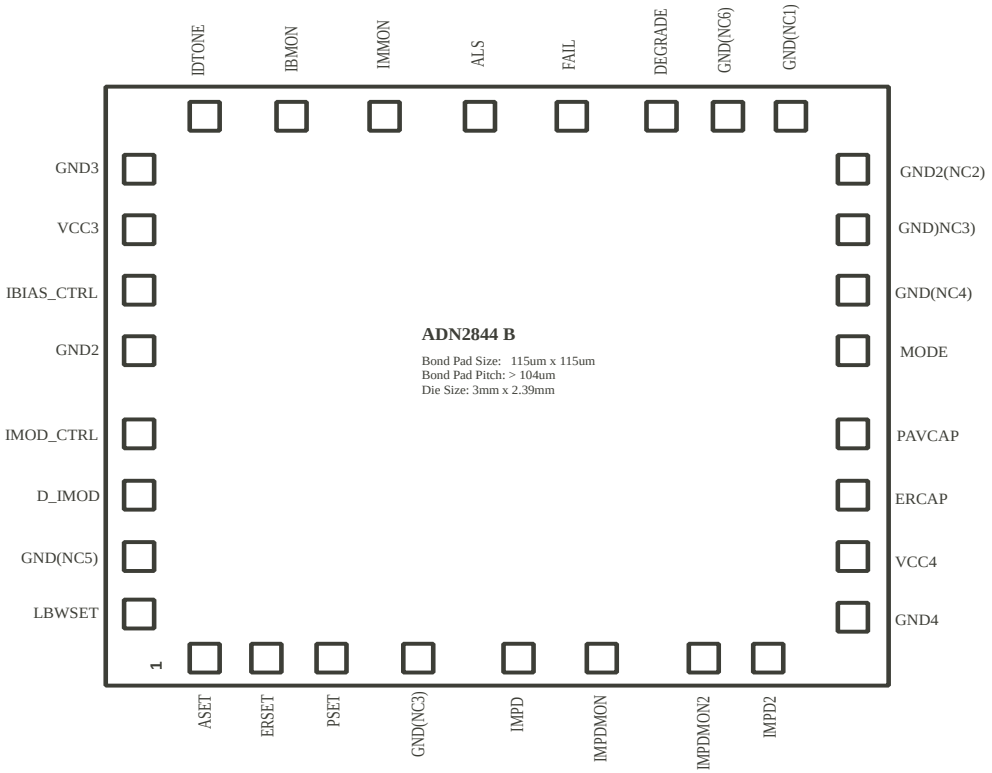
$$Icc=75mA+1.75xI_{MOD}(mA)+0.3xI_{BIAS}(mA)$$

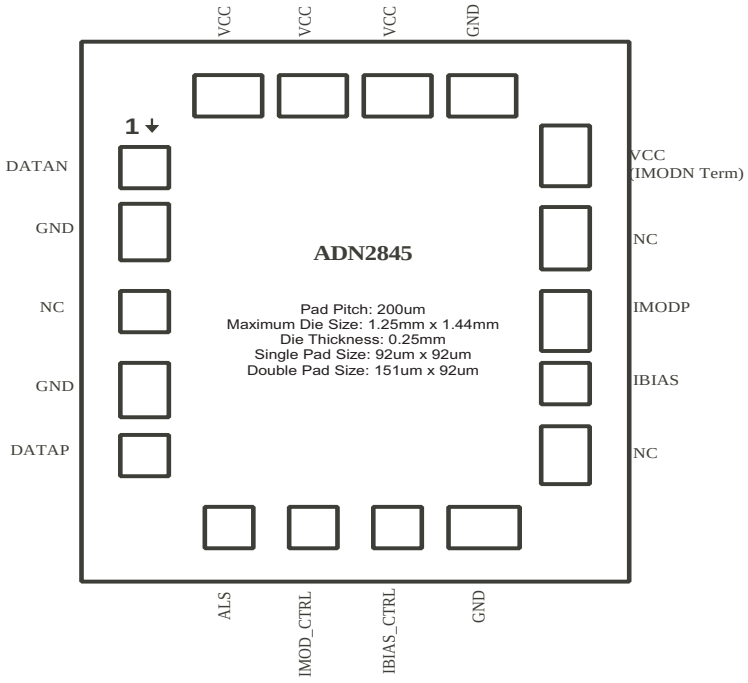
$$P=Vcc\ x\ Icc\ +V_{IMOD}\ x\ I_{MOD}(A)/2\ +\ V_{IBIAS}\ x\ I_{BIAS}(A)$$

where V_{IMOD} is the average voltage on the IMOD pin, and V_{IBIAS} is the average voltage on the IBIAS pin.

PACKAGE OUTLINE

Both the ADN2844 and the ADN2845 are available as bare die.
The ADN2844 is also available in 5mmx5mm 32 pin LFCSP.

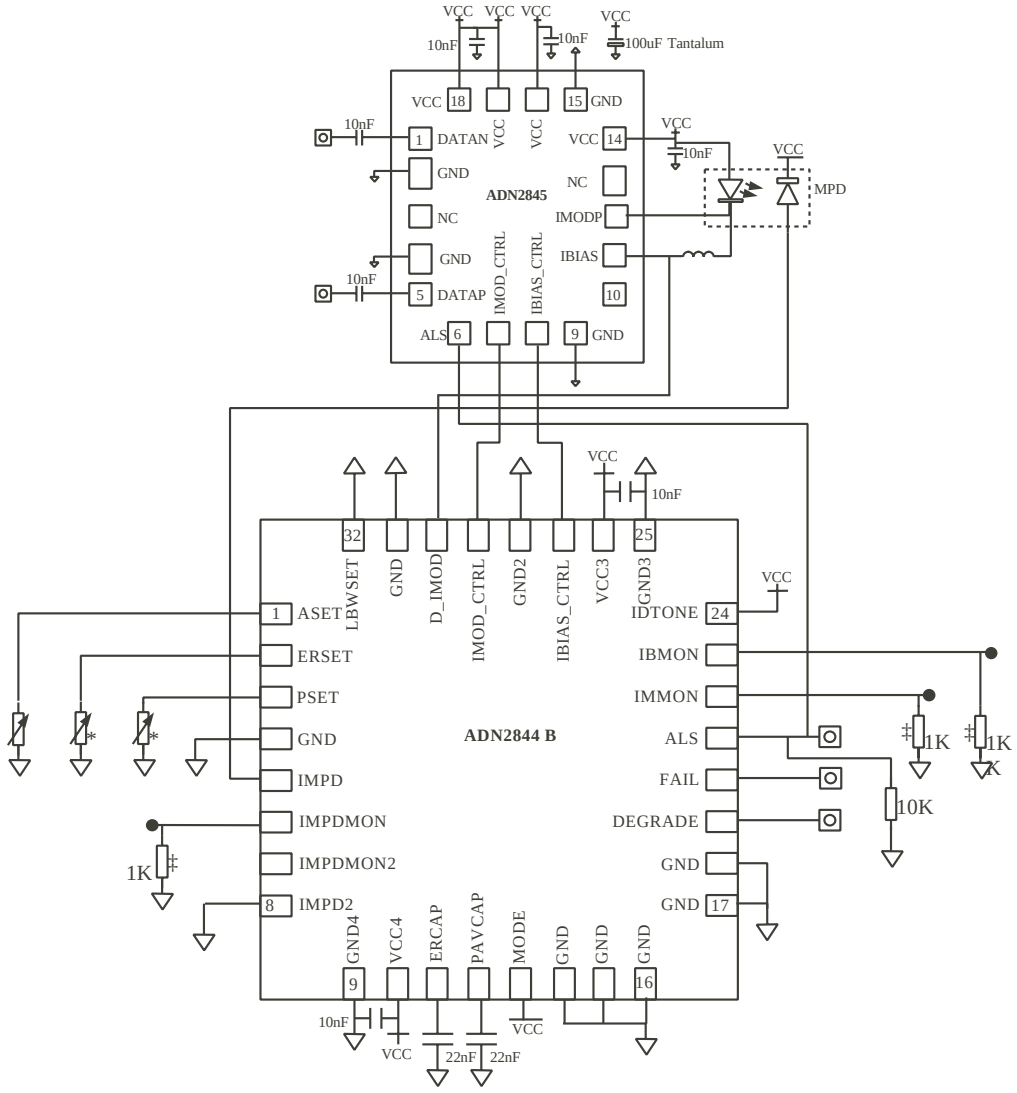




PIN FUNCTION DESCRIPTION

PIN	ADN2844B	FUNCTION
1	ASET	Alarm current threshold set
2	ERSET	Extinction Ratio Current Set
3	PSET	Average Optical Power set pin
4	GND	Test Input(nc8)
5	IMPD	Monitor Photo Diode current input
6	IMPDMON	Mirrored current from IMPD
7	IMPDMON2	Mirrored current from IMPD2 (For optional use with twoMPDs)
8	IMPD2	Optional second MPD current input
9	GND4	Negative supply
10	VCC4	Positive supply
11	ERCAP	Extinction Ratio loop capacitor
12	PAVCAP	Avearge Power Loop capacitor
13	MODE	Control loop operating mode logic input
14	GND	Test Input (nc4)
15	GND	Test Input (nc3)
16	GND	Test Input (nc2)
17	GND	Test Input (nc1)
18	GND	Test Input (nc6)
19	DEGRADE	DEGRADE Alarm output, open collector, active high
20	FAIL	FAIL Alarm output, open collector, active high
21	ALS	Automatic Laser Shutdown Logic Input
22	IMMON	Modulation current mirror putput, current source from Vcc
23	IBMON	Bias current mirror output, current source from Vcc
24	IDTONE	ID Tone input current
25	GND3	Negative supply
26	VCC3	Positive supply
27	IBIAS_CTRL	Control output current sink
28	GND2	Negative supply
29	IMOD_CTRL	Control output current sink
30	D_IMOD	Control output current sink
31	GND	Test Input (nc5)
32	LBWSET	Select Low Loop Bandwidth Mode (Active = Vcc)

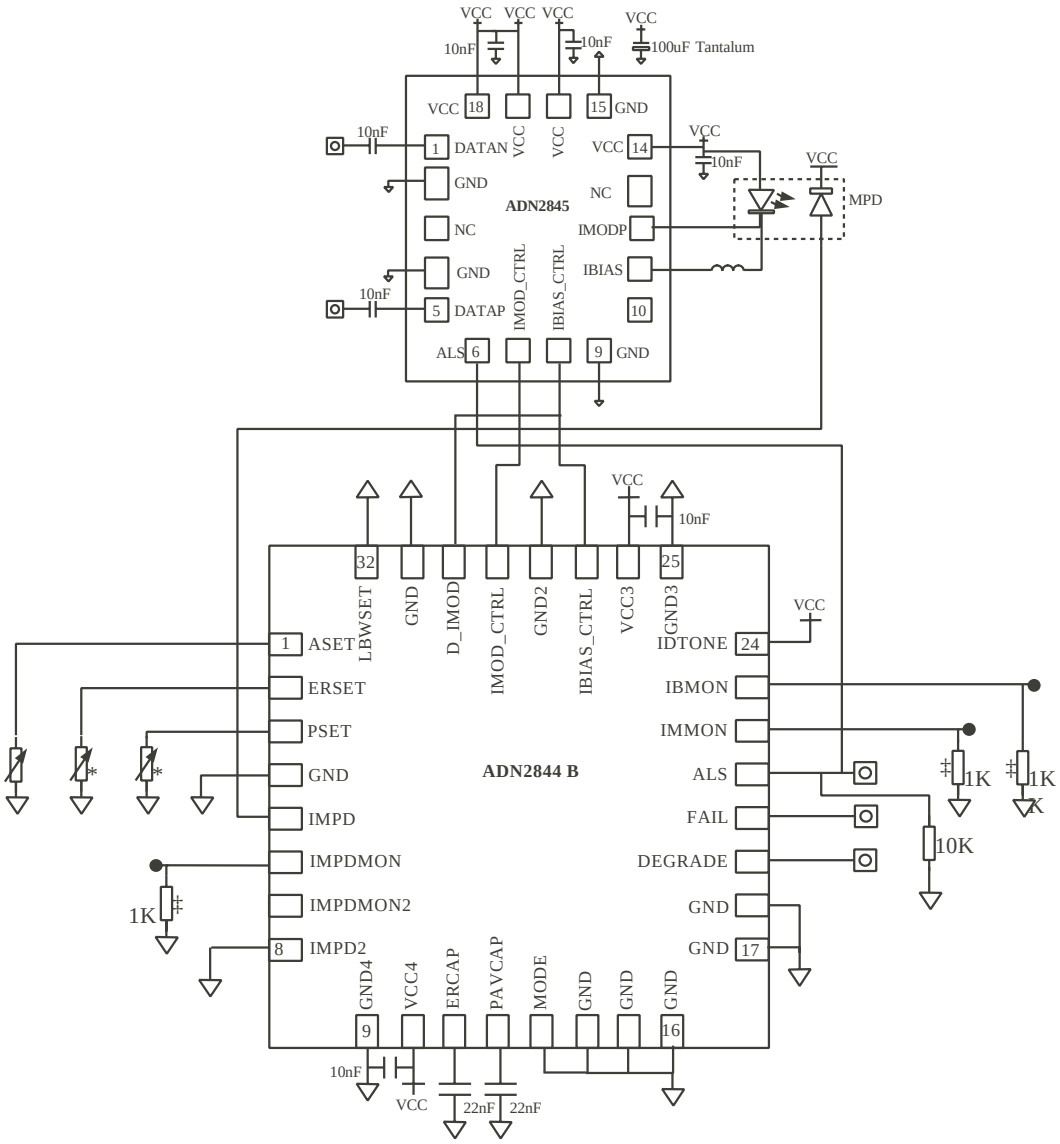
PIN	ADN2845	FUNCTION
1	DATAN	AC Coupled CML Data, negative differential terminal
2	GND	Negative supply
3	NC	No connect - leave floating
4	GND	Negative supply
5	DATAP	AC Coupled CML Data, positive differential terminal
6	ALS	Automatic LAser Shutdown Logic Input
7	IMOD_CTRL	Modulation current control input (Control circuit sinks IMOD/10 from pin to GND)
8	IBIAS_CTRL	BIAS current control input (Control Circuit sinks IBIAS/10 from pin to GND)
9	GND	Negative supply
10	NC	No Connect - leave floating
11	IBIAS	BIAS current
12	IMODP	Modulation current
13	NC	No connect - leave floating
14	VCC	VCC connection for IMODN termination resistor
15	GND	Negative supply
16	VCC	Positive supply
17	VCC	Positive supply
18	VCC	Positive supply



* For digital programming, the ADN2850 optical supervisor can be used
‡ Optional monitoring of currents

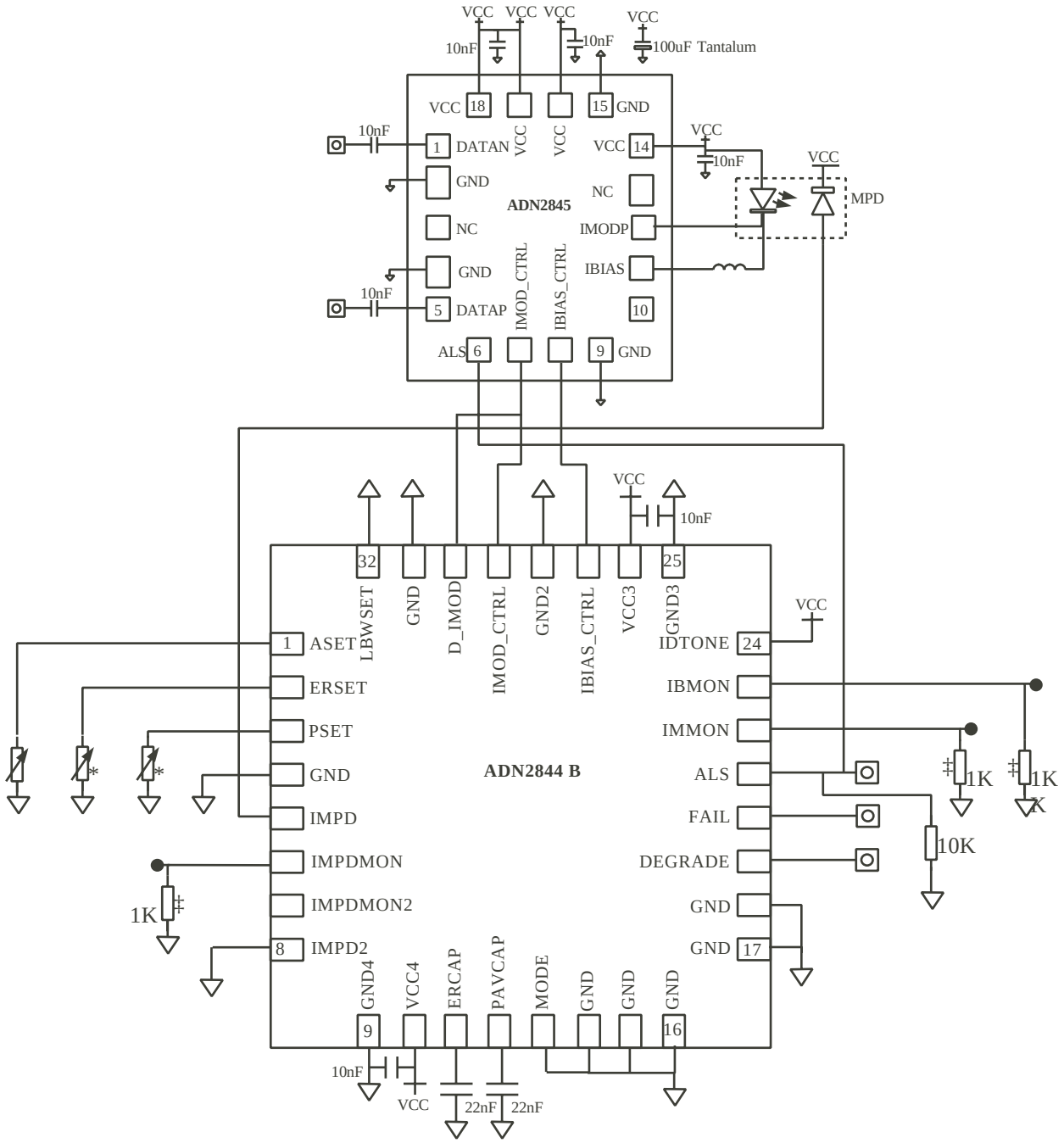
Figure 2. ADN2843 application circuit (mode A)

- Best high frequency board layout techniques including power and ground planes should be used.
- To minimize inductance, keep the connections between the ADN2845 and the laser diode as short as possible.
- Place bypass capacitor on laser anode as close to laser as possible.
- Minimise bond lengths for ADN2845 pads to achieve low inductance.
- Ribbon bonding can be used to reduce bond inductance.
- Critical bonds are IMODP and VCC (pin 14).
- Connecting to ADN2845 GND (pin 13) is optional if it allows inductance on VCC (pin 14) to be further reduced.
- Bypass capacitors should be placed as close as possible to VCC pads.
- 50Ω controlled impedance interconnects should be used on the DATA inputs
- Value of the AC coupling capacitors on the DATA inputs depends on the frequency content of the data
- Parasitic capacitance on IBIAS_CTRL and IMOD_CTRL interconnects should be less than 100pF. If decoupling caps are used on IBIAS_CTRL and IMOD_CTRL, they should be tied to VCC rather than GND.
- A ferrite of type Murata BLM11HA601SG is recomended for IBIAS inductor on ADN2845



* For digital programming, the ADN2850 optical supervisor can be used
‡ Optional monitoring of currents

Figure 3. ADN2843 application circuit (mode B)



* For digital programming, the ADN2850 optical supervisor can be used
‡ Optional monitoring of currents

Figure 4. ADN2843 application circuit (mode C)

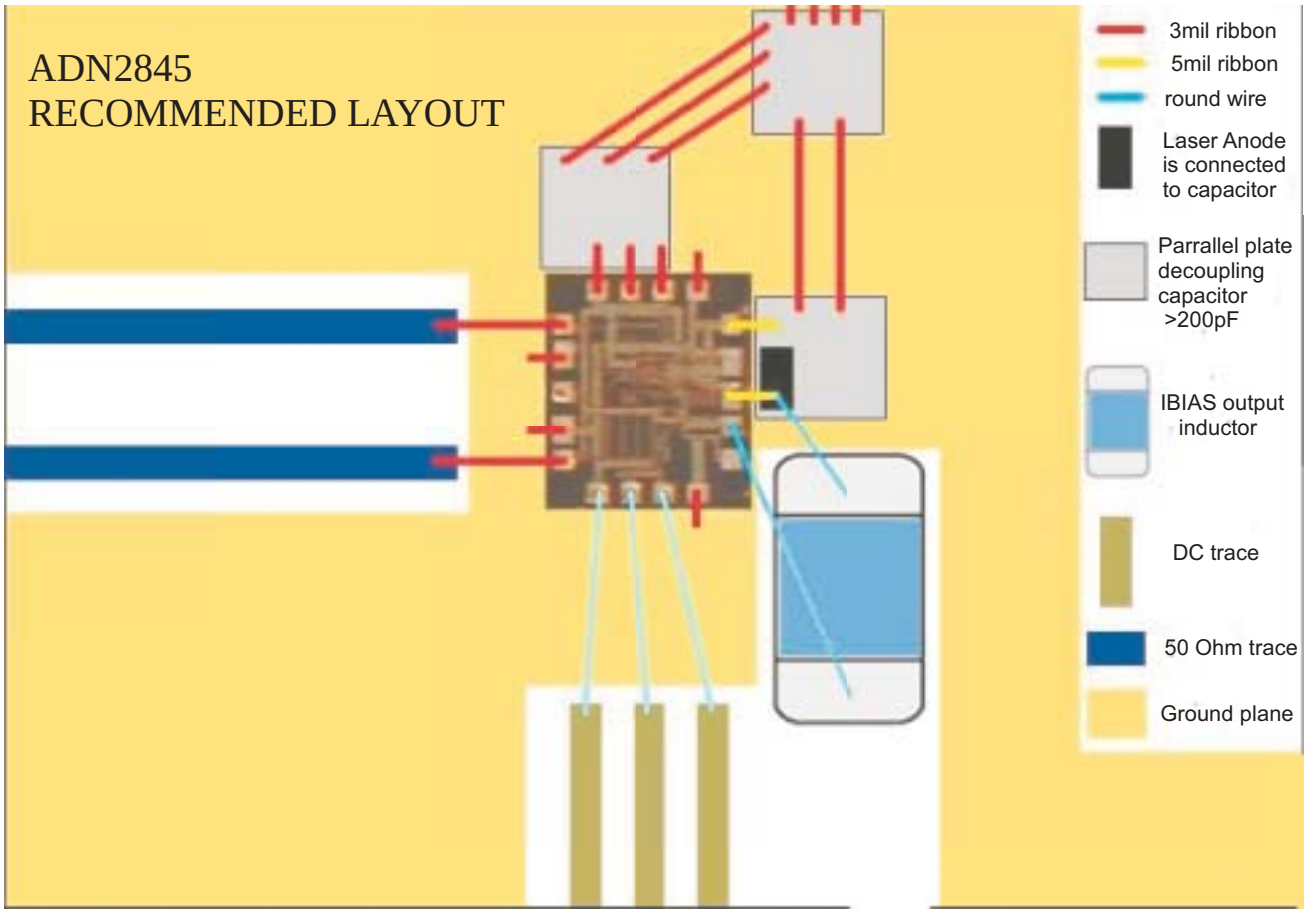


Figure 5. ADN2845 - recommended layout

Diepad Coordinates

(with origin in the center of the die)

ADN2845

Pad #	Pad Name	X [µm]	Y [µm]
1	DATAN	-500.00	400.00
2	GND**	-500.00	222.00
3	NC	-500.00	0.00
4	GND**	-500.00	-222.00
5	DATAP	-500.00	-400.00
6	ALS	-300.00	-600.00
7	IMOD_CTRL	-100.00	-600.00
8	IBIAS_CTRL	100.00	-600.00
9	GND**	300.00	-600.00
10	NC**	500.00	-400.00
11	IBIAS	500.00	-200.00
12	IMODP**	500.00	-30.00
13	NC**	500.00	178.00
14	VCC(IMODN)**	500.00	378.00
15	GND**	300.00	600.00
16	VCC**	100.00	600.00
17	VCC**	-100.00	600.00
18	VCC**	-300.00	600.00

***** denotes double bondpad***

ADN2844

Pad #	Pad Name	X [µm]	Y [µm]
1	ASET	1014.00	-1019.00
2	ERSET	769.00	-1019.00
3	PSET	486.00	-1019.00
4	GND	186.00	-1019.00
5	IMPD	-132.00	-1019.00
6	IMPDMON	-479.00	-1019.00
7	IMPDMON2	-811.00	-1019.00
8	IMPD2	-1056.00	-1019.00
9	GND4	-1339.00	-877.00
10	VCC4	-1339.00	-672.00
11	ERCAP	-1339.00	-429.00
12	PAVCAP	-1339.00	-204.00
13	MODE	-1339.00	91.00
14	GND	-1339.00	335.00
15	GND	-1339.00	580.00
16	GND	-1339.00	824.00
17	GND	-1051.00	1019.00
18	GND	-761.00	1019.00
19	DEGRADE	-476.00	1019.00
20	FAIL	-207.00	1019.00
21	ALS	102.00	1019.00
22	IMMON	387.00	1019.00
23	IBMON	653.00	1019.00
24	IDTONE	904.00	1019.00
25	GND3	1359.00	995.00
26	VCC3	1359.00	781.00
27	IBIAS_CTRL	1359.00	523.00
28	GND2	1359.00	317.00
29	IMOD_CTRL	1359.00	-29.00
30	D_IMOD	1359.00	-294
31	GND	1359.00	-562.00
32	LBWSET	1359.00	-807.00